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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/006,516	12/03/2001	Kuang Chi	01-51	8011

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LATTICE SEMICONDUCTOR CORPORATION
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EXAMINER	
GHULAMALI, QUTBUDDIN	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

CT

Office Action Summary	Application No.	Applicant(s)	
	10/006,516	CHI ET AL.	
	Examiner	Art Unit	
	Qutub Ghulamali	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-21,26 and 27* is/are allowed.

6)☒ Claim(s) *22-24 and 28-32* is/are rejected.

7)☒ Claim(s) *25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/11/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 22 rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (US Patent 6,122,336) in view of Aung et al (US Pub. 2003/0212930).

Regarding claim 22, Anderson discloses a Digital clock recovery circuit for generating a recovered clock signal comprising:

a phase detector (fig. 2, element 202) operable to compare a serial data input (SDIN) with a recovered clock signal (SCLK) and to generate in response up and down signals (col. 3, lines 9-13);

a phase selector (206) operable to select a clock signal as the recovered clock signal (SCLK) from a plurality of given clock signals (2N clock) in response to FWD (forward) and BWD (backward) signals (col. 3, lines 11-20); and

a digital filter (204) coupled between the phase detector (202) and the phase selector (206), the digital filter (204) operable to generate the FWD and BWD signals for the phase selector in response to the up and down signals (212, 214) received from the phase detector (202) (col. 3 lines 15-30). However, Anderson is silent regarding the specific details of the digital filter.

In the same field of endeavor, Aung discloses a clock data recovery circuit, wherein the digital filter includes at least one reloadable register (multi stage shift register 200) (figs. 1-5) operable to store a programmable value for comparison (110; col. 3, section 0044) with a value derived from the up and down signals and a controller responsive to the comparison and operable to generate the FWD and BWD signals (col. 5, sections 0060, 0061). It would have been obvious to one skilled in the art at the time the invention was made to use shift registers to store programmable values for comparison with a derived value from the up and down signals to generate signals as taught by Aung in the clock recovery circuit of Anderson so as create perfect synchronism with the clock signal information embedded in the CDR.

Regarding claim 23, Anderson and Aung in combination disclose every feature of the claimed invention in claim 22. However, Aung further discloses the DPLL is part of a data recovery circuit within a SERDES (serializer/deserializer) transceiver (fig. 10, elements 340b, 60b).

Regarding claim 24, Anderson and Aung in combination disclose every feature of the claimed invention in claim 22. Aung, however, further discloses (fig. 4), a phase interpolator (162) coupled to a multiplexer (190) responsive to the FWD and BWD signals, the multiplexer operable to receive a plurality of given clock signals having different phases as inputs and to select each of at least two clock signals as one of the given clock signals as outputs, the phase interpolator operable to generate the recovered clock signal (SCLK) having a phase that is phase interpolated between the phases of the at least two selected clock signals (col. 4, sections 0052, 0053, 0054).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 28-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Anderson.

Regarding claims 28 and 32, Anderson discloses a digital clock recovery circuit comprising:

comparing a serial data input (SDIN) with a recovered clock signal (SCLK) and generating in response up and down signals (col. 3, lines 9-13);

deriving a value from the up and down signals (col. 3, lines 14-30);

comparing a programmable (predefined) value with the derived value (col. 3, lines 10-14);

generating FWD (forward) (advance) and BWD (backward) (retard) signals in response to the comparison of the programmable value and derived value (col. 3, lines 20-30); and

selecting a clock signal as the recovered clock signal (SCLK) from a plurality of given clock signals in response to the FWD and BWD signals (col. 3, lines 28-30).

Regarding claim 29, Anderson discloses (fig. 2), selecting at least two clock signals from a plurality of given clock signals (abstract; 2N clocks) having different phases in response to the FWD and BWD signals (fig. 4, col. 3, lines 66-67; col. 4, lines 1-2); and

generating the recovered clock signal (SCLK) having a phase that is phase interpolated between the phases of the at least two selected clock signals (col. 4, lines 2-11).

Regarding claims 30 and 31, Anderson discloses deriving a value from the up and down signals comprises generating a value representing a difference and sum between counts of up and down signals pulses (col. 4, lines 55-67).

Allowable Subject Matter

5. Claim 25 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claim 1-21, 26-27 allowed.

Reasons for allowance

7. The following is an examiner's statement of reasons for allowance:

With reference to claims 1, 8, 15, the prior art fails to teach or suggest, alone or in combination a digital filter of a DPLL (Digital Phase locked loop) comprising:
a first reloadable register portion for storing a TBW (total bandwidth) value, wherein said first reloadable register portion is capable of being coupled to a first port for inputting said TBW value that is programmed into said first reloadable register portion through said first port;
a second reloadable register portion for storing a DBW (differential bandwidth) value, wherein said second reloadable register portion is capable of being coupled to a second port for inputting said DBW value that is programmed into said second reloadable register portion through said second port;

an up_counter for generating an UP_CNT value by counting up each UP signal pulse generated by a phase transition detector when a first phase of a SDTN (serial data input) signal leads a second phase of a current ACLK (recovered clock) signal generated by a phase selector;

a down counter for generating a DOWN_CNT value by counting up each DOWN signal pulse generated by said phase transition detector when said first phase of said SDTN (serial data input) signal lags said second phase of said current ACLK (recovered clock) signal;

an adder for adding said UP_CNT value and said DOWN_CNT value to generate a SUM value;

a subtractor for generating a DELTA value that is the difference between said UP_CNT value and said DOWN_CNT value;

a delta comparator for asserting a LTP (larger than positive) signal if the magnitude of said DELTA value is greater than said DBW value and if said DOWN_CNT value is greater than said UP_CNT value, and for asserting a STN (small than negative) signal if the magnitude of said DELTA value is greater than said DBW value and if said UP_CNT value is greater than said DOWN_CNT value;

a sum comparator for asserting a WE (write enable) signal when said SUM value is greater than said TBW value; and

a phase select controller for asserting a FWD (forward) signal if said LTP signal is asserted when said WE signal is asserted or for asserting a BWD (backward) signal if said STN signal is asserted when said WE signal is asserted; wherein said phase selector selects another clock signal having a leading phase from said current ACLK signal as a new ACLK (recovered clock) signal when said FWD signal is asserted;

and wherein said phase selector selects another clock signal having a lagging phase from said current ACLK signal as said new ACLK (recovered clock) signal when said BWD signal is asserted;

and wherein said phase selector selects said current ACLK signal to remain as said new ACLK (recovered clock) signal if said FWD signal and said BWD signal are not asserted when said WE signal is asserted.

Such limitations as recited in the independent claims 1, 8 and 15, are neither anticipated nor rendered obvious by the prior art.

Regarding claim 26, the prior art fails to teach or suggest, alone or in combination, a digital filter comprising:

at least two reloadable registers, each operable to store a programmable value;

a subtractor operable to generate a value representing a difference between counts of received up and down signal pulses;

an adder operable to generate a value representing a sum of counts of the received up and down signal pulses;

a first comparator coupled to a first reloadable register and to the subtractor and operable to generate a signal based on comparison of the first register's programmable value and the difference value;

a second comparator coupled to a second reloadable register and to the adder and operable to generate a signal based on comparison of the second register's programmable value and the sum value; and

a controller responsive to the signals generated by the first and second comparators and operable to generate FWD and BWD signals.

Such limitations as recited in the independent claim 26, is neither anticipated nor rendered obvious by the prior art.

Claims 2-7, 9-14, 16-21, and 27 are allowed by virtue of their dependency to claims highlighted above.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patents:

Fraisse (US Patent 6,041,080) shows a signal processing system receives and mixes a plurality of analog signals.

Saitoh et al (US Patent 5,604,775) discloses a digital phase looked loop with coarse delay line and phase detector delivers clock pulses.

Fisher et al (US Pub. No. 2002/0027886) shows a method for controlling data sample clocking of nodes in a frame based communications network.

Mallory (US Pub. No. 2002/0042836) discloses a method for enhancing network transmission in a communications system.

Shin (US 5,991,341) shows TCM decoder of HDTV receiver with clock and data recovery portion.

Publications:

Romdhane, M.S.B.; Madisetti, V.K.; "LMSGEN: a prototyping environment for programmable adaptive digital filters in VLSI" VLSI Signal Processing, VII, 1994., [Workshop on] , 26-28 Oct. 1994 Pages 33 – 42.

Kwan, H.K.; "Tunable and variable passive digital filters for multimedia signal processing" Intelligent Multimedia, Video and Speech Processing, 2001. Proceedings of 2001 International Symposium on, 2-4 May 2001 Pages 229 – 232.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutub Ghulamali whose telephone number is (571) 272-3014. The examiner can normally be reached on Monday-Friday from 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QG.
February 24, 2005.

JAY K. PATEL
SUPERVISORY PATENT EXAMINER